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Applicant(s): Y. AJIOKA, et al

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For: VISUAL DEVICE

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents
Washington, D.C. 20231

March 9, 2001

Sir:

In the matter of the above-identified application, applicant(s) is/are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the application papers accompanying this Information Disclosure Statement.

To the extent that, the documents listed on the attached form equivalent to Form PTO-1449, are not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by the "A concise explanation of relevancy" attached hereto.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1089.39666X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

Melvin Kraus
Registration No. 22,466
ANTONELLI, TERRY, STOUT & KRAUS, LLP

MK/cee
Attachments
(703) 312-6600

A concise explanation of relevancy

1. A counter of the number of parking cars, Published Unexamined Japanese Patent Application No. H5-324954.

   Summary

   The counter in this patent application couts the number of parking cars, by extracting edges of the parking cars in some judgement region in a parking shown in Fig.2 (page 2 column 2 line 17–page 2 column 2 line 20).

   Comparison

   (a) The counter in this patent application uses a well-known methods as the method for extracting edges (page 2 column 2 line 17–page 2 column 2 line 20). Therefore, the method for extracting edges in this patent application can not genenrate edge information of moving objects on outdoors, where there is much noise.

   (b) The counter in this patent application counts the number of parking cars, based on the edges extracted on the assumption of the form of the cars. On the other hand, the visual device can count the number of objects even though their form is not fixed like amoebas. Both, therefore, are not same.

2. An image processing and analyzing device of a fluid, Published Unexamined Japanese Patent Application No. H7-175934.

   Summary

   The image processing and analyzing device in this patent application analyzes flow of the fluid, carrying out the process shown in Fig.4 (page 3 column 2 line 29–page 4 column 1 line 46).

   Comparison

   (a) In the image processing and analyzing device in this patent application, it is clear that the process of calcuration is not equivalent to Fig.4(d) if the concentration of the fluid is not uniform. The image processing and analyzing device in this patent application, therefore, can not genenrate edge information of moving objects on outdoors, where there is much noise.

   (b) The image processing and analyzing device in this patent application can not analyze the flow of the fluid when Oil Myst is stacked. On the other hand, the visual device can count the number of the objects even though the objects are stacked. Both, therefore, are not same.

3. A display system of a varying image, Published Unexamined Japanese Patent Application No. S61-206079.

   Summary

   The display system in this patent application carries out Affine transformation shown in Equation 1, by using array processors shown in Fig.1 (page 442 column 1 line 6–page 442 column 3 line 10).

   Comparison

(a) The display system in this patent application carries out Affine transformation, by offering a whole image to all processing elements via video bus (page 440 column 1 line 14–page 440 column 3 line 11, Fig.1). Each processing element segments an image region, which should be processed by itself, by a window, followed by rotating (page 442 column 2 line 1–page 442 column 3 line 10, Fig.6). On the other hand, the visual device takes an image, in which the size of objects is suitable, by controlling a moving camera (Fig.6). In addition, the geometrical analyzis means carries out global processing like Fourier transform and Hough transform (Description, page 59 line 20–page 60 line 21, Fig.12). Both, therefore, are not same.

4. A. Tojo, Pattern Description with a Highly Parallel Information Processing System I, Denkishikenjo Ihou, Vol.31, No.8, pp.18-34, 1967.

Summary

This paper reports a method converting a quantized figure to description by combinations of special points and sequences of line segments in terms of highly parallel information processing, in order to describe figures in a figure discription language (page 24 column 2 line 9–page 31 column 2 line 15). Main parallel operations are described as follows:

(a) Smoothing (page 26 column 2 line 5–page 27 column 1 line 30)

(b) Making a diagram (page 27 column 1 line 31–page 27 column 1 line 30)

(c) Extracting a terminal point (page 29 column 2 line 6–page 29 column 2 line 25)

(d) Extracting a cross point (page 29 column 2 line 16–page 30 column 1 line 1)

(e) Extracting an edge point (page 30 column 1 line 2–page 30 column 1 line 17)

(f) Differentiation of a diagram (page 30 column 1 line 18–page 31 column 1 line 8)

These operations are carried out by a 3x3 matrix or its combination (page 28 column 1 line 1–page 28 column 1 line 21). The highly parallel information processing system comprises some n x m processing cells, each of which has a one or two-bit register and carries out propagation, matching by a 3x3 matrix, transmission, an AND operation, an OR operation and so on (page 31 column 2 line 16–page 33 column 1 line 2).

Comparion

(a) Although a target in this paper is only a operation represented by a 3x3 matrix or its combination, the invention of the visual device carries out more than or equal to eight neighbor processing. The highly parallel information processing system in this paper, therefore, can not carry out the figure/ground separation means, the position/size detection means and so on in the invention of the visual device.

(b) In this paper, each cell is connected with eight neighbors. On the other hand, in the invention of the visual device, each array operation unit is connected with four neighbors, and transmits calcuration data via its controler. The array operation unit, therefore, deals with any neighbor domain in a simple transmit rule and with a less volume of hardware than the cell in this paper.

5. A. Tojo, T. Yamaguchi, H. Aoyama, Pattern Description with a Highly Parallel Information Unit (VI) –Construction and Simulation of the System–, Denkishikenjo Ihou, Vol.33, No.5, pp.1-27, 1969.

   Summary

   This paper reports a detail of hardware of the highly parallel information system (page 2 column 1 line 38–page 8 column 2 line 3). The highly parallel information system offers data to each cell by `D_REGISTER` (page 4 column 1 line 2–page 4 column 1 line 9), and controls a communication direction by controling communication paths by `R_REGISTER` (page 4 column 1 line 10–page 4 column 1 line 22, Fig.2). Operations carreid out by the highly parallel information system are described as follows:

   (a) 3x3-matrix matching (page 3 column 1 line 1–page 4 column 1 line 22)
   (b) 3x3-matrix operation in an OR form (page 4 column 1 line 23–page 4 column 2 line 15)
   (c) propagation (page 4 column 2 line 16–page 5 column 1 line 8)
   (d) plane boolean operation (page 5 column 1 line 9–page 5 column 1 line 29)

   Comparion

   (a) Although propagation carried out by the highly parallel information system in this paper propagates "1" information which a cell has in any successive domain, all array operation units send their calcuration data to the whole of their neighbors which are decided beforehand in the invention of the visual device. Particularly, in the invention of the visual device, the array operation unit, which behaves as a MIMD-type processor, can determine timing according to judgement of itself, and transmit data efficently (Description, page 111 line 25–page 118 line 9). Both, therefore, are not same.

6. Shigeo Ohyagi, Ryoichi Mori, Atsuhito Kobayashi, Shoji Watanabe, Recognition of Hand-printed Japanese Characters Called "HIRAGANA" Using Local Parallel Operations, Technical Report of the Institute of Electronics and Comunication Engineers, IE76-87, pp.11-18, 1976.

   Summary

   The system in this paper recognizes HIRAGANA by carrying out feature detection, the porinomial matching and the strict matching, on the assumption of use of array processors. Each processing is described as follows:

   (a) Feature detection using the graph theory and the field effect method (page 12 column 2 line 1–page 13 column 1 line 15)

(b) porinomial matching (page 14 column 1 line 1–page 15 column 1 line 15)
(c) strict matching (page 15 column 1 line 16–page 16 column 2 line 3)

Array Processors realize the field effect method by local and parallel processing, but are used to solve simultaneous equations in transforming input figures in the porinomial matching (page 12 column 1 line 1–page 12 column 1 line 44).

Comparison

(a) The field effect method in this paper can also be carried out by the array operation units in the invention of the visual device.
(b) The system in this paper calcurates feature points and transforms figures in order to matching a diagram. On the other hand, in the invention of the visual device, the area normalization means calcurates gravity of neighbors every pixel, and transfers each pixel in the opposite direction to the gravity (Description, page 90 line 4–page 94 line 4, Fig.24). The invention of the visual device, therefore, can carry out pattern matching of a face which lies at any position in a color image (Description, page 96 line 9–page 101 line 18, Fig.27).

7. M.J.B. Duff, CLIP-4: A Large Scale Integrated Circuit Array Parallel Processor, Proc. 3rd IJCPR, pp.728-733, 1976.

Comparison

(a) Since each cell in CLIP-4 has to operate while its neighbor cells output binary data simultaneously (page 729 column 2 line 14–page 729 column 2 line 56, Fig.3), the cell can not communicate the binary data exactly if the cells do not send and receive the data synchronously each other. On the other hand, in the invention of the visual device, since the controler in each array operation unit can communicate asynchronously (Description, page 115 line 17–page 115 line 23), the array operation unit can receive calcuration data whenever it is possible for the Unit to receive them. Therefore, CLIP-4 is a SIMD-type multi-processor system, all of whose cells execute the same instruction simultaneously, while the visual device is a MIMD-type multi-processor system, wherein each of the array operation units work freely. Particularly, it is really difficult to increase clock frequency because the larger the scale of circuits becomes corresponding to the size of an image, the more difficult the SIMD-type multi-processor offers a synchronous signal to all processors. The invention of the visual device, however, can increase the clock frequency more easily than CLIP-4.
(b) Each cell in CLIP-4 is physically connected with eight neighbors in this paper. Since the cell does not have a function for transmitting data to the neighbors, the cell can not carry out neighbor processing using more than eight neighbors. The cell, therefore, must increase the number of connections corresponding to the number of the neighbors, in order to compute each equation in the invention of the visual device.
(c) A target of CLIP-4 in this paper is only binary data. Since there are no functions representing binary data in the bit-serial form, CLIP-4 can not

deal with some byte data. CLIP-4, therefore, must be appended some capacity of memory and synchronous mechanism for bit-serial data, corresponding to the number of the necessary bits, in order to compute each equation in the invention of the visual device.

8. Kenneth E. Batcher, MPP: A High-speed Image Processor, Algorithmically Specialized Parallel Computers, pp.59-68, 1985.

   Comparison

   (a) Although the MPP in this paper is a SIMD-type multi-processor system (page 59 line 22–page 59 line 27), the visual device is a MIMD-type multi-processor system (Description, page 111 line 25–page 118 line 17). Both, therefore, are not same.

   (b) Since a SPE in this paper can not set TYPE and transfer region of calcuration data (Fig.2), it can not examine algorithms of the visual device.

9. N. Takahashi, M. Amamiya, A Data Flow Processor Array System Design and Analysis, Proc. 10th ISCA, 1983.

   Comparison

   (a) Although the system in this paper uses some data flow processors (page 244 column 1 line 42–page 244 column 2 line 12), the visual device can use some general purpose processors and some simple controlers managed by the processors (Description, page 111 line 25–page 113 line 21). The system in this paper, therefore, is expensive.

   (b) Since the system in this paper uses the data flow processor, the processor executes computation quickly when the processor receives data. On the other hand, in the invention of the visual device, the processor must supervise reception of data (Description, page 117 line 20–page 118 line 9). In this paper, therefore, the processor can execute a program efficently, while the processor in the visual device needs a program for transmitting data and executing computation efficently.

   (c) In this paper, since the processor is the data flow processor, the processor must complete transmitting the necessary data before executing computation (Fig.2) although it is difficult for the processor to predict the order of computation executed really. The processor then needs mechanism for checking arrival of data (page 246 column 1 line 29–page 246 column 2 line 15). On the other hand, in the visual device, the processor can give priority to transmission of data over execution of computation by a program. In this paper, therefore, unless a programmer investigates the order of executing a program carefully or an application like scientific problems, whose results do not change in spite of varying the order of execution a little, is selected, followed by generation of efficent codes by a compiler, the system can not really execute the program in parallel efficently. On the other hand, in the visual device, the processor can carry out local and parallel processing efficently in spite of the order of transmission of data, by giving a top priority to sharing data in the neighbors.

10. Masatoshi Ishikawa, A Method for Measuring the Center Position and the Total Intensity of an Output Distribution of Matrix Positioned Sensors, Journal of the Society of Instrument and Control Engineers, Vol.19, No.5, pp.23-28, 1983.

Summary

This paper describes means for computing the central position of a two-dimensional pattern within a certain domain and its summation in parallel (page 210 column 2 line 5–page 213 column 2 line 9).

Comparison

(a) Although analog circuits in this paper can not derive the central position of only one pattern and its summation simultaneously, the position/size detection means in the visual device can detect position and size of some areas represented by line segments consisting of edge information simultaneously (Description, page 86 line 11–page 89 line 14, Fig.21).

11. Toshiharu Mukai, Masatoshi Ishikawa, Two-dimensional Coordinates Transform Circuit for Parallel Processing Vision, IPSJ Technical Report, Computer Vision, 80-28, pp.209-214, 1992.

Summary

This paper describes a means for computing the central posiiton of a two-dimensional pattern within a certain domain on any nonlinear coordinate and its summation in parallel (page 210 column 2 line 5–page 213 column 2 line 9).

Comparison

(a) Although analog circuits in this paper can not derive the central position of only one pattern and its summation simultaneously, the position/size detection means in the visual device can detect position and size of some areas represented by line segments consisting of edge information simultaneously (Description, page 86 line 11–page 89 line 14, Fig.21).

12. Takashi Komuro, Idaku Ishii, Masatoshi Ishikawa, Vision Chip Architecture Using General-Purpose Processing Elements for 1ms Vision System, Proc. 4th IEEE Int. workshop on Computer Architecture for Machine Perception (CAMP'97), pp.276-279, 1987.

Comparison

(a) Architecture of a vision chip in this paper, S^3PE, is a SIMD-type multiprocessor system arranging processing elements, which communicate and compute data in the bit-serial form, in the form of a lattice (Fig.1). On the other hand, the visual device is a MIMD-type multi-processor system wherein each array operation unit works freely. S^3PE is suitable for executing only one algorithm processing binary data since S^3PE desires less volume of hardware of a processor itself than the visual device. Architecture of the visual device, however, excels more than S^3PE, in terms of the volumn of hardware for sending control signals to each processor, design of timing of digital circuits, computational period, data transmission period and parallel execution of many algorithm in the processor.

(b) In S^3PE in this paper, since each processing element is physically connected to only four neighbors, the element must transmit data as the invention of the visual device does in order to communicate to more than four neighbors. However, since S^3PE is the SIMD-type multi-processor system, all processing elements can not transmit the data to only one neighbor element simultaneously. Then, in a case that the domain of the neighbors becomes a little more than four neighbors, the efficency of transmission of data comes to extremely low. Therefore, if S^3PE is going to compute equations in the invention of the visual device, it takes much time for communication. On the other hand, in the invention of the visual device, since the controler can send calcuration data to a combination of any of four neighbors (Description, page 114 line 20–page 115 line 15), each array operation unit can scatter one of calcuration data to any neighbors in short period. The array operation unit, therefore, can use communication paths connected to only four neighbors efficently.

13. Yoshihiro Nakabo, Idaku Ishii, Masatoshi Ishikawa, 1ms Target Tracking System Using Massively Parallel Processing Vision, Journal of the Robot Society of Japan, Vol.15, No.3, pp.105-109, 1997.

Summary

A tracking system in this paper controls the direction of a camera within one millisecond of cycle time, by using SPE-256 which arranges 16x16 SPEs, shown in Fig.3 (page 106 column 1 line 23–page 107 column 1 line 17, Fig.1, Fig.2).

Comparison

(a) Although the system in this paper tracks a bright object quickly, the visual device carries out finding objects, separating the objects from background, normalization, recognition, counting and generation of an environmental map.

(b) Although the SPE-256 in this paper is a SIMD-type multi-processor system (page 106 column 1 line 30–page 106 column 1 line 36), the visual device is a MIMD-type multi-processor system (Description, page 111 line 25–page 118 line 17). Both, therefore, are not same.

(c) Althgouh the system in this paper can process only an binary image (page 106 column 2 line 4–page 106 column 2 line 12), the visual device generates edge information from color images (Description, page 76 line 12–page 80 line 21).

(d) Since a SPE in this paper can not set TYPE and transfer region of calcuration data (Fig.3), it can not examine algorithms of the visual device.

14. Takashi Komuro, Shinsuke Suzuki, Idaku Ishii, Masatoshi Ishikawa, Design of Massively Parallel Vision Chip Using General-Purpose Processing Element, Journal of the Institute of Electronics, Information and Communication Engineers, Vol.J81-D-I, No.2, pp.70-76, 1998.

Summary

A tracking system in this paper controls the direction of a camera within one

millisecond of cycle time, by using S^3PE shown in Fig.1.

Comparison

(a) Although the system in this paper tracks a bright object quickly, the visual device carries out finding objects, separating the objects from background, normalization, recognition, counting and generation of an environmental map.

(b) Although the S^3PE in this paper is a SIMD-type multi-processor system (page 71 column 1 line 21–page 71 column 1 line 42), the visual device is a MIMD-type multi-processor system (Description, page 111 line 25–page 118 line 17). Both, therefore, are not same.

(c) Although a PE in this paper carries out bit-serical operations (page 72 column 2 line 1–page 73 column 1 line 15, Table 1), the visual device can execute operations fast by using general-purpose processors.

(d) Since the PE in this paper can not set TYPE and transfer region of calcuration data (Fig.2), it can not examine algorithms of the visual device.

15. Ch. von Malsburg, W. Schneider, A Neural Cocktail-Party Processor, Biol. Cybern. Vol.54, pp.29-40, 1986.

Comparison

(a) Although each excitatory unit in a network in this paper has a global connection (page 31 column 1 line 1–page 31 column 1 line 33, Fig.2), each nonlinear oscillator in the figure/ground separation means in the visual device is connected to only neighbors (Description, page 102 line 14–page 103 line 7).

(b) In the network in this paper, all excitatory units are classified into two sets of their phases (page 35 column 2 line 8–page 36 column 2 line 16, Fig.8), but they can not separate some object areas from background by using edge information. Moreover, the network does not have a function complementing rough edge information.

16. Christoph von Malsburg, Joachim Buhmann, Sensory segmentation with coupled neural oscillators, Biol. Cybern. Vol.67, pp.233-242, 1992.

Comparison

(a) Although each excitatory unit in a network in this paper has a global connection (page 239 column 2 line 1–page 240 column 1 line 2, Fig.5), each nonlinear oscillator in the figure/ground separation means in the visual device is connected to only neighbors (Description, page 102 line 14–page 103 line 7).

(b) In the network in this paper, all excitatory units are classified into two sets of their phases (page 35 column 2 line 8–page 36 column 2 line 16, Fig.8), but they can not separate some object areas from background by using edge information. Moreover, the network does not have a function complementing rough edge information.

17. Thomas B. Schillen, Peter König, Binding by temporal structure in multiple feature domains of an oscillatory neural network, Biol. Cybern. Vol.70, pp.397-405, 1994.

Comparison

(a) Since an oscillator in this paper is connected to the nearest neighbors and other neighbors by two kinds of links whose delay times are different each other, respectively, synchronization and desynchronization are realized by the links (page 398 column 2 line 42–page 399 column 1 line 3, Fig.1). On the other hand, in the figure/ground separatin means in the visual device, a nonlinear oscillator is connected to its neighbors according to the near excitatory and far inhibitory rule (Description, page 102 line 14–page 103 line 7). The connection of the visual device, therefore, is simpler than this paper.

(b) Disparity level of an image is given to the oscillator in this paper as a stimulus (page 399 column 2 line 4–page 399 column 2 line 14, Fig.2B). On the other hand, in the figure/ground means in the visual device, formed edge information controls a link between the oscillators (Description, page 103 line 8–page 104 line 3). Therefore, although the network in this paper does not need a special pretreatment, the network segments many areas without limitation when an real image is inputed to it. On the other hand, the figure/ground means desires the edge-information generation means and the edge-information formation means.

(c) Although the oscillator in this paper distinguishes some areas by a combination of its amplitude and its phase (page 399 column 2 line 21–page 400 column 1 line 19, Fig.2C, Fig.2D), some areas are represented by the phase in the figure/ground separation means (Description, page 108 line 7–page 110 line 20). It is, therefore, suitable for the network in this paper to segment many fragmental areas, but it is suitable for the visual device to separate human faces from a real environment.

18. David Terman, DeLiang Wang, Global competition and local cooperation in a network of neural oscillators, Physica, D, 81, pp.148-176, 1995.

Comparison

(a) After each pixel of an binary image is converted to a positive or negative number, the number is given to an oscillator in this paper (page 154 column 1 line 36–page 154 column 1 line 41). On the other hand, formed edge information controls a link between oscillators in the figure/ground separation means in the visual device (Description, page 103 line 8–page 104 line 3). Therefore, although a network in this paper does not need a special pretreatment, the network can not segment some areas exactly when an real image is inputed to it. On the other hand, the figure/ground means desires the edge-information generation means and the edge-information formation means.

(b) In the network in this paper, each oscillator is connected to a global inhibitor by a global link (page 152 column 1 line 16–page 153 column 2 line

13, Fig.4). On the other hand, in the figure/ground separation means in the visual device, each nonlinear oscillator is connected to its neighbors (Description, page 102 line 14–page 103 line 7).

(c) The network in this paper can extract some areas individually by using the global inhibitor, even though the areas are not concatenated (page 169 column 1 line 23–page 171 column 2 line 16). On the other hand, in the figure/ground separation means in the visual device, the areas are not be divided fragmently because the number of the areas is assigned within a certain range (Description, page 108 line 7–page 110 line 20).

19. K. Kyuma, E. Lange, J. Ohta, A. Hermanns, B. Banish, M. Oita, Artificial Retinas–Fast, Versatile Image Processing, Nature, 372, 6502, pp.197-198, Nov. 1994.

Comparison

(a) The artificial retinas in this paper is fundamentally a sequential machine. Note that the Pixel Array can carry out an operation for a row or a column of a taken image collectively if the operation is simple as output control. On the other hand, in the invention in the visual device, each array operation unit has a processor and can perform operation individually (Description, page 111 line 25–page 112 line 23). The artificial retinas, therefore, can not carry out local and parallel processing in the visual device efficently.

(b) Since the artificial retinas in this paper can carry out Fourier transform for only a specific spatial frequency toward a horizontal direction and a vertical direction, the artificial retinas can output only horizontal and vertical line segments rather than performs pattern matching (Fig.2e). In addition, since the artificial retinas calcurates a histgram toward the vertical direction, and a neural network specially carries out character recognition for a result of the histgram, the artificial retinas is weak for position gap of the image, and is not suitable for recognizing many characters (page 197 column 3 line 7–page 197 column 3 line 31, Fig.2f). On the other hand, in the invention in the visual device, since the area normalization means normalizes an object area into the size of image (Description, page 90 line 4–page 94 line 4, Fig.24, Fig.25), and the image recognition means carries out pattern matching every pixel (Description, page 96 line 9–page 101 line 18, Fig.27, Fig.28), the visual device can recognize some similar objects at unspecific places.

20. R. Colin Johnson, Vision Chip's Circuitry Has Its Eye Out For You, Techweb News, `http://www.techweb.com/wire/news/1997/09/0913vision.html`, 1997.

Comparison

(a) The GVPP in this article adjusts brightness and extracts edges (page 1 line 35–page 1 line 41).

(b) Each neuron of the GVPP in this article has only a RAM, a few registers, an adder and a comparator. The GVPP, therefore, can not carry out algorithms of the visual devices in parallel.

Form PTO-1449 Equivalent	U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 1089.39666X00 Serial No. (not yet assigned) Applicant: Y. AJIOKA Filing Date: Group:

U.S. Patent Documents

Examiner Initials	Document No.	Date	Name	Class	Subclass	Filing Date If Approp.

Foreign Patent Documents

Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No
61-206079	9/86	Japan				
5-324954	12/93	Japan				
7-175934	7/95	Japan				

Other Documents (including Author, Title, Date, Pertinent Pages, etc.)

"Pattern Description with a Highly Parallel Information Processing System I", A. Tojo, Denkishikenjo Ihou, Vol. 31, No. 8, pp. 18-34, 1967

"Pattern Description with a Highly Parallel Information Unit (VI)-Construction and Simulation of the System", A. Tojo et al, Denkishikenjo Ihou, Vol. 33, No. 5, pp. 1-27, 1969

"Recognition of Hand-Printed Japanese Characters Called HIRAGANA Using Local Parallel Operations, S. Ohyagi, et al, Technical Report of the Institute of Electronics and Communication Engineers, IE76-87, pp. 11-18, 1976

"CLIP-4: A Large Scale Integrated Circuit Array Parallel Processor", MJB Duff, Proc. 34d IJCPR, pp.728-733, 1976

"MPP: A High-Speed Image Processor, Algorithmically Specialized Parallel Computers", Kenneth E. Batcher, pp. 59-68, 1985

"A Data Flow Processor Array System Design and Analysis", N. Takahashi et al, Proc. 10th ISCA, 1983

"A Method for Measuring the Center Position and the Total Intensity of an Output Distribution of Matrix Positioned Sensors", M. Ishikawa, Journal of the Society of Instrument and Control Engineers, Vol. 19, No. 5, pp. 23-28, 1983

Other Documents (including Author, Title, Date, Pertinent Pages, etc.)

"Two-Dimensional Coordinates Transform Circuit for Parallel Processing Vision", T. Mukai et al, IPSJ Technical Report, Computer Vision, 80-28, pp. 209-214, 1992

"Vision Chip Architecture Using General-Purpose Processing Elements for 1ms Vision System", T. Komuro et al, Proc. 4th IEEE Int. Workshop on Computer Architecture for Machine Perception (CAMP'97), pp. 276-279, 1987

"1 ms Target Tracking System Using Massively Parallel Processing Vision", Y. Nakabo et al, Journal of the Robot Society of Japan, Vol. 15, No. 3, pp. 105-109, 1997

"Design of Massively Parallel Vision Chip Using General-Purpose Processing Element", T. Komuro et al, Journal of the Institute of Electronics, Information and Communication Engineers, Vol. J81-D-I, No. 2, pp. 70-76, 1998

"A Neural Cocktail-Party Processor", C. von Malsburg et al, Biol. Cybern., Vol. 54, pp.29-40, 1986

"Sensory Segmentation with Coupled Neural Oscillators", C. von Malsburg et al, Biol. Cybern, Vol. 67, pp.233-242, 1992

"Binding by Temporal Structure in Multiple Feature Domains of an Oscillatory Neural Network", T. Schillen et al, Biol. Cybern., Vol. 70, pp. 397-405, 1994

"Global Competition and Local Cooperation in a Network of Neural Oscillators", D. Terman et al, Physica, D, 81, pp. 148-176, 1995

"Artificial Retinas-Fast, Versatile Image Processing", K. Kyuma et al, Nature, 372, 6502, pp. 197-198, Nov. 1994

"Vision Chip's Circuitry has its Eye Out for You", R. Johnson, Techweb News

Examiner Date Considered

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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.